AMENDMENTS TO THE SPECIFICATION:

Page 16 (as amended 7/6/2005): please replace paragraph 0030 with the following amended paragraph:

In some embodiments, the sleep mode voltage controller 140 may provide the array high supply voltage V_{ADD}, the array low supply voltage V_{ASS} and the well voltage at optimum values for a set of transistor parameters. For example, the sleep mode voltage controller 140 may provide the array high supply voltage V_{ADD} at about 0.8 volts, the array low supply voltage V_{ASS} at about 0.4 volts and the n-well voltage V_{nwell} at about 1.2 volts for a general technology class of transistors. Thus, the SRAM array may have about 0.4 volts back bias on both the n-channel and the p-channel in addition to about 0.4 volts across the SRAM cell, as shown in FIGURES 4 and 5. As shown in FIG. 5, this embodiment provides a well voltage such that an n-channel back bias voltage, a p-channel back bias voltage, and a voltage across the SRAM cell are about (but probably not exactly) the same.